

What is claimed is:

1           1.     An etching process for use in manufacturing a semiconductor device,  
2     comprising:  
3           forming a first layer on a semiconductor substrate;  
4           forming a polysilicon hard mask on the first layer, the polysilicon hard mask  
5     having a pattern such that a portion of the first layer is exposed;  
6           dry etching the exposed portion of the first layer using the polysilicon hard  
7     mask as an etching mask to form an opening in the first layer; and  
8           supplying an etching gas onto the polysilicon hard mask in a direction  
9     substantially parallel to the major upper surface of the semiconductor substrate to  
10    thereby dry etch the polysilicon hard mask.

1           2.     The process of claim 1, and further comprising forming a conductive  
2     layer on the semiconductor substrate, and wherein the forming of the first layer  
3     comprises forming a dielectric film on the conductive layer.

1           3.     The process of claim 1, wherein the dry etching of the first layer forms  
2     an opening which exposes the surface of the semiconductor substrate, and further  
3     comprising subsequently etching the exposed portion of the semiconductor  
4     substrate to form a trench in the semiconductor substrate.

1           4.     The process of claim 1, wherein the supplying of an etching gas  
2     comprises supplying an etching gas which reacts with the silicon of the polysilicon  
3     hard mask.

1           5.     The process of claim 1, wherein the supplying of an etching gas  
2     comprises supplying a fluorine-containing compound.

1           6.     The process of claim 5, wherein the etching gas comprises at least one  
2     halogen fluoride selected from the group consisting of ClF, ClF<sub>3</sub>, BrF, BrF<sub>3</sub>, BrF<sub>5</sub>, IF,  
3     IF<sub>3</sub> and IF<sub>5</sub>.

1           7.     The process of claim 5, wherein the etching gas comprises XeF<sub>2</sub>.

1           8.     The process of claim 1, wherein the dry etching of the polysilicon hard  
2 mask comprises supplying the etching gas along with a carrier gas.

1           9.     The process of claim 8, wherein the carrier gas is one of nitrogen and  
2 argon.

1           10.    The process of claim 1, wherein the dry etching of the polysilicon hard  
2 mask comprises rotating the semiconductor substrate while the polysilicon hard  
3 mask is exposed to the etching gas.

1           11.    The process of claim 1, wherein the dry etching of the polysilicon hard  
2 mask comprises supplying the etching gas in a series of pulses of a predetermined  
3 period.

1           12.    The process of claim 11, wherein the dry etching of the polysilicon hard  
2 mask is carried out at a pressure of at most several tens of mTorr.

1           13.    The process of claim 11, wherein the dry etching of the polysilicon hard  
2 mask is carried out at room temperature.

1           14.    The process of claim 11, wherein the dry etching of the polysilicon hard  
2 mask comprises rotating the semiconductor substrate while the polysilicon hard  
3 mask is exposed to the etching gas.

1           15.    An apparatus for use in manufacturing a semiconductor device,  
2 comprising:  
3           a reaction chamber comprising a casing, and a spin chuck disposed within  
4 said casing, said spin chuck being configured to support a semiconductor substrate  
5 and being rotatable, whereby a semiconductor substrate supported thereon can be  
6 rotated;

7           a gas supply unit connected to said reaction chamber, said gas supply unit  
8           supplying the reaction chamber with a process gas for removing unnecessary  
9           material from a semiconductor substrate mounted to the spin chuck in the reaction  
10          chamber;

11          a gas injection unit connecting said gas supply unit to said reaction chamber,  
12          said gas injection unit having at least one gas injection opening, each said at least  
13          one gas injection opening being oriented such that the gas injection unit injects the  
14          process gas, supplied by the gas supply unit, into the reaction chamber in a  
15          horizontal direction substantially parallel to the major upper surface of a  
16          semiconductor substrate mounted to the spin chuck in the reaction chamber, and  
17          an exhaust unit connected to said reaction chamber so as to exhaust gases  
18          from the reaction chamber.

1           16.    The apparatus of claim 15, wherein said gas supply unit comprises a  
2           source of a fluorine-containing gaseous compound.

1           17.    The apparatus of claim 16, wherein the compound is a gas selected  
2           from the group consisting of ClF, ClF<sub>3</sub>, BrF, BrF<sub>3</sub>, BrF<sub>5</sub>, IF, IF<sub>3</sub>, IF<sub>5</sub> and XeF<sub>2</sub>.

1           18.    The apparatus of claim 16, wherein said gas supply unit further  
2           comprises a source of a carrier gas.

1           19.    The apparatus of claim 15, wherein said gas injection unit is disposed  
2           on an inner side wall of said casing of the reaction chamber, and comprises a  
3           shower head having a plurality of gas injection openings through which the process  
4           gas flows into the reaction chamber in a horizontal direction above said spin chuck.

1           20.    The apparatus of claim 15, and further comprising a puff valve  
2           connected in-line between said gas supply unit and said reaction chamber, said puff  
3           valve being operative to supply the process gas flowing from the gas supply unit into  
4           the reaction chamber as a series of pulses of a predetermined period.